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2. The method of Claim 1, wherein the steps of inputting the generalized failure data to a circuit analysis tool and obtaining from the circuit analysis tool first localized probable defect data are performed ~~substantially~~^{continuously} using at least one programmed computer.

4. The method of Claim 1, wherein the integrated circuits are logic ~~circuits~~ ^{having} built-in self-test capabilities.

6. The method of Claim 5, wherein the integrated circuits are tested in wafer form.

7. The method of Claim 1, wherein obtaining from the circuit analysis ~~first~~ ^{first} localized probable defect data comprises:

creating a database against which the logic defect data is processed to obtain physical defect data; and

processing the logical defect data against the database to obtain physical defect data.

8. The method of Claim 7, wherein creating the database comprises translating design information from a first format to a second format.

29. A system for testing semiconductor integrated circuits, comprising:
a circuit analysis tool; and
means for automatically;

applying to the/circuit analysis tool generalized failure data;

obtaining from the circuit analysis tool localized probable defect data;

representing the localized probable defect data in a standard format;

and

storing the localized probable defect data on a database server accessible to multiple client machines.

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Sub. 13/2

14